

NPN SILICON RF POWER TRANSISTOR

DESCRIPTION:

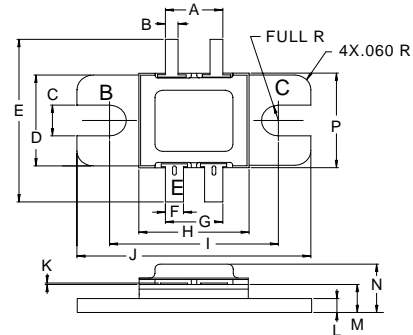
The **AUR500** is designed for high peak power & low duty cycle applications, in the 400-500 MHz.

FEATURES:

- Internal Input Matching Network
- $P_G = 9.5$ dB at 500 W/500 MHz
- **Omnigold™** Metalization System
- Emitter Ballasting
- Common Base

MAXIMUM RATINGS

I_C	43.2 A
V_{CBO}	65 V
V_{CES}	65 V
V_{EBO}	3.5 V
P_{DISS}	1167 W @ $T_C = 25$ °C
T_J	-65 °C to +200 °C
T_{STG}	-65 °C to +150 °C
θ_{JC}	0.15 °C/W

PACKAGE STYLE .400 BAL FLG (A)


DIM	MINIMUM inches / mm	MAXIMUM inches / mm
A	.210 / 5.33	.230 / 5.84
B	.045 / 1.14	.055 / 1.40
C	.125 / 3.18	.135 / 3.43
D	.380 / 9.65	.390 / 9.91
E	.770 / 19.56	.830 / 21.08
F	.070 / 1.78	.080 / 2.03
G	.215 / 5.46	.235 / 5.97
H	.420 / 10.67	.430 / 10.92
I	.645 / 16.38	.655 / 16.64
J	.895 / 22.73	.905 / 22.99
K	.002 / 0.05	.006 / 0.15
L	.058 / 1.47	.065 / 1.65
M	.115 / 2.92	.130 / 3.30
N		.230 / 5.84
P	.395 / 10.03	.405 / 10.29

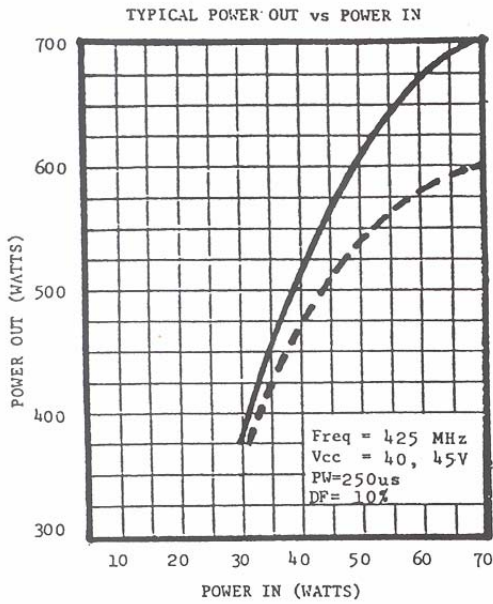
ORDER CODE: ASI10550
CHARACTERISTICS $T_C = 25$ °C

SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
BV_{CBO}	$I_C = 50$ mA	65			V
BV_{CES}	$I_C = 50$ mA	65			V
BV_{EBO}	$I_E = 10$ mA	3.5			V
I_{CBO}	$V_{CB} = 30$ V			15	mA
h_{FE}	$V_{CE} = 5.0$ V $I_C = 5.0$ A	00		200	---
P_G	$V_{CC} = 40$ V $P_{OUT} = 500$ W $f = 425$ MHz	9.5			dB
η_C		50			%

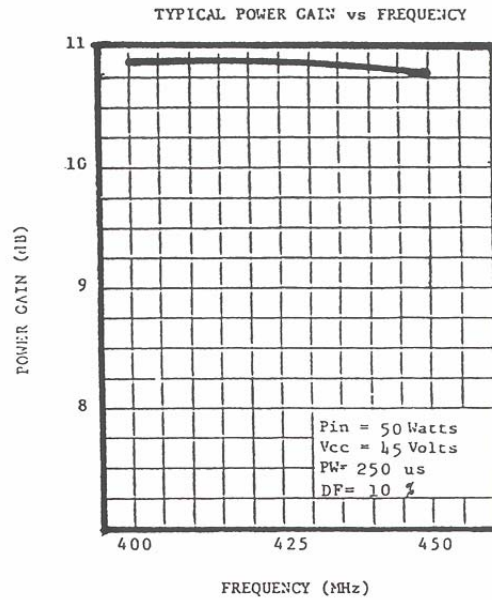
 NOTE: Pulse Width = 250 μ S. Duty Cycle = 10%

TYPICAL PERFORMANCE

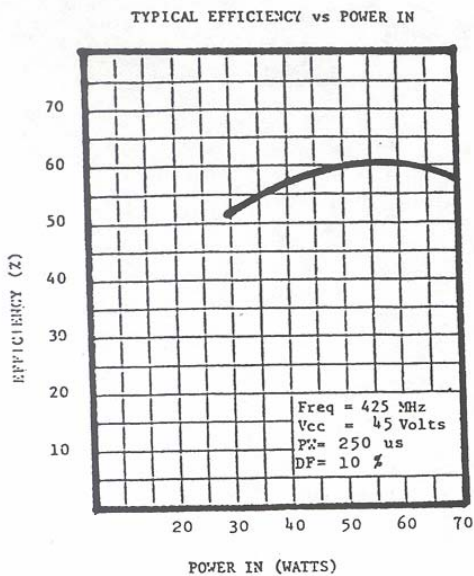
POWER OUTPUT vs POWER INPUT



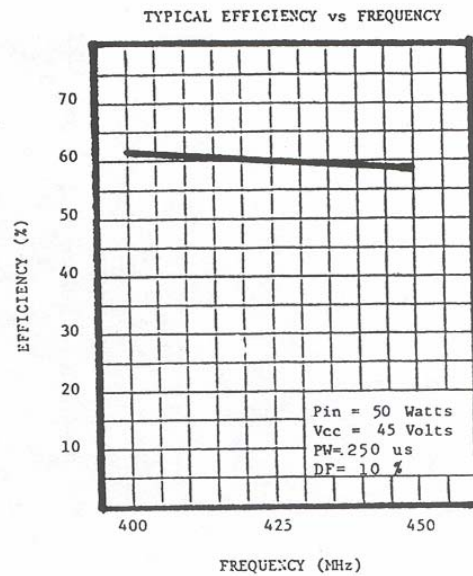
POWER GAIN vs FREQUENCY



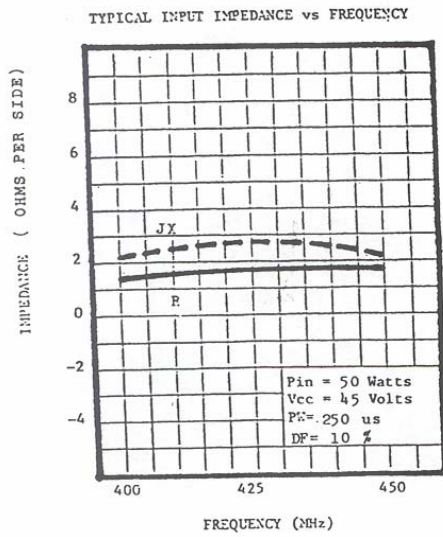
EFFICIENCY vs POWER INPUT



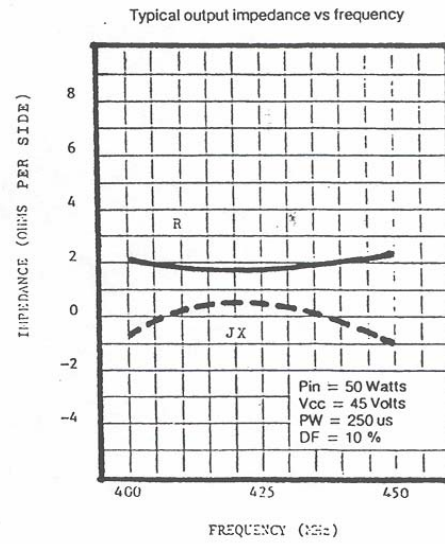
EFFICIENCY vs FREQUENCY



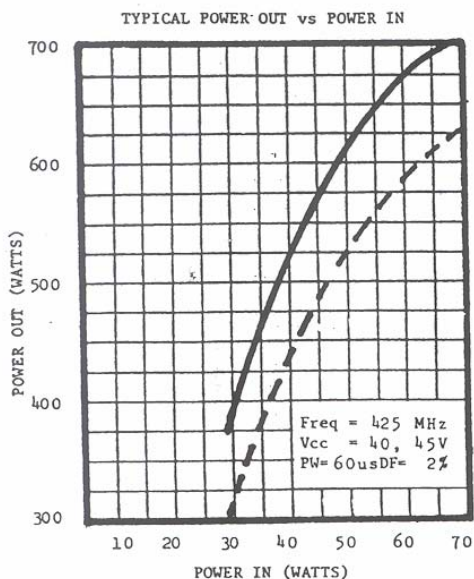
TYPICAL INPUT IMPEDANCE



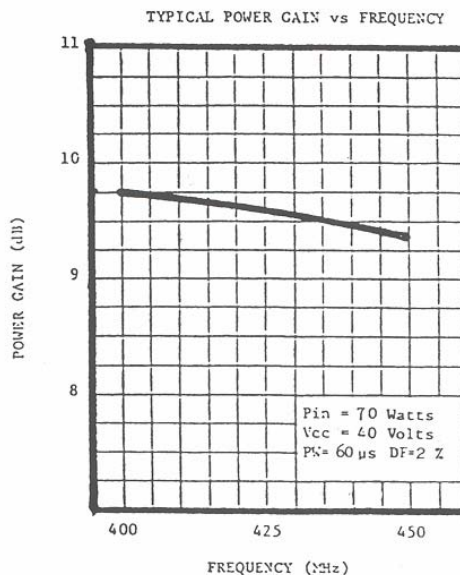
TYPICAL COLLECTOR LOAD IMPEDANCE



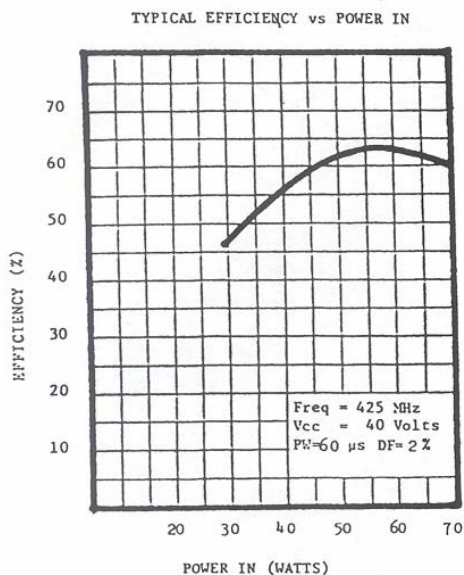
POWER OUTPUT vs POWER INPUT



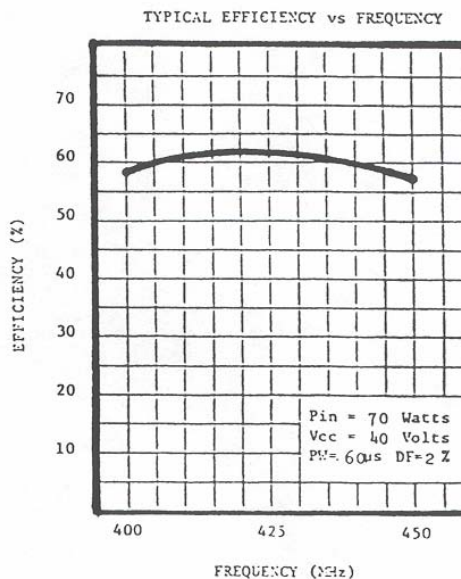
POWER GAIN vs FREQUENCY



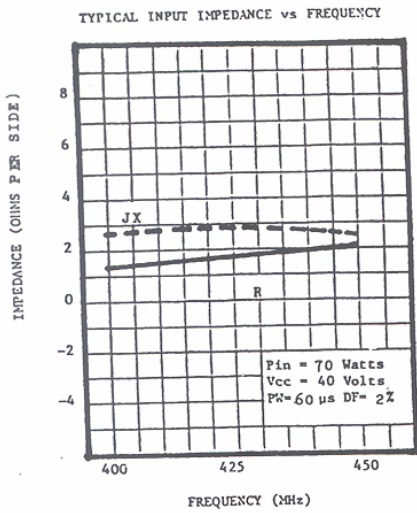
EFFICIENCY vs POWER INPUT



EFFICIENCY vs FREQUENCY



TYPICAL INPUT IMPEDANCE



TYPICAL COLLECTOR LOAD IMPEDANCE

